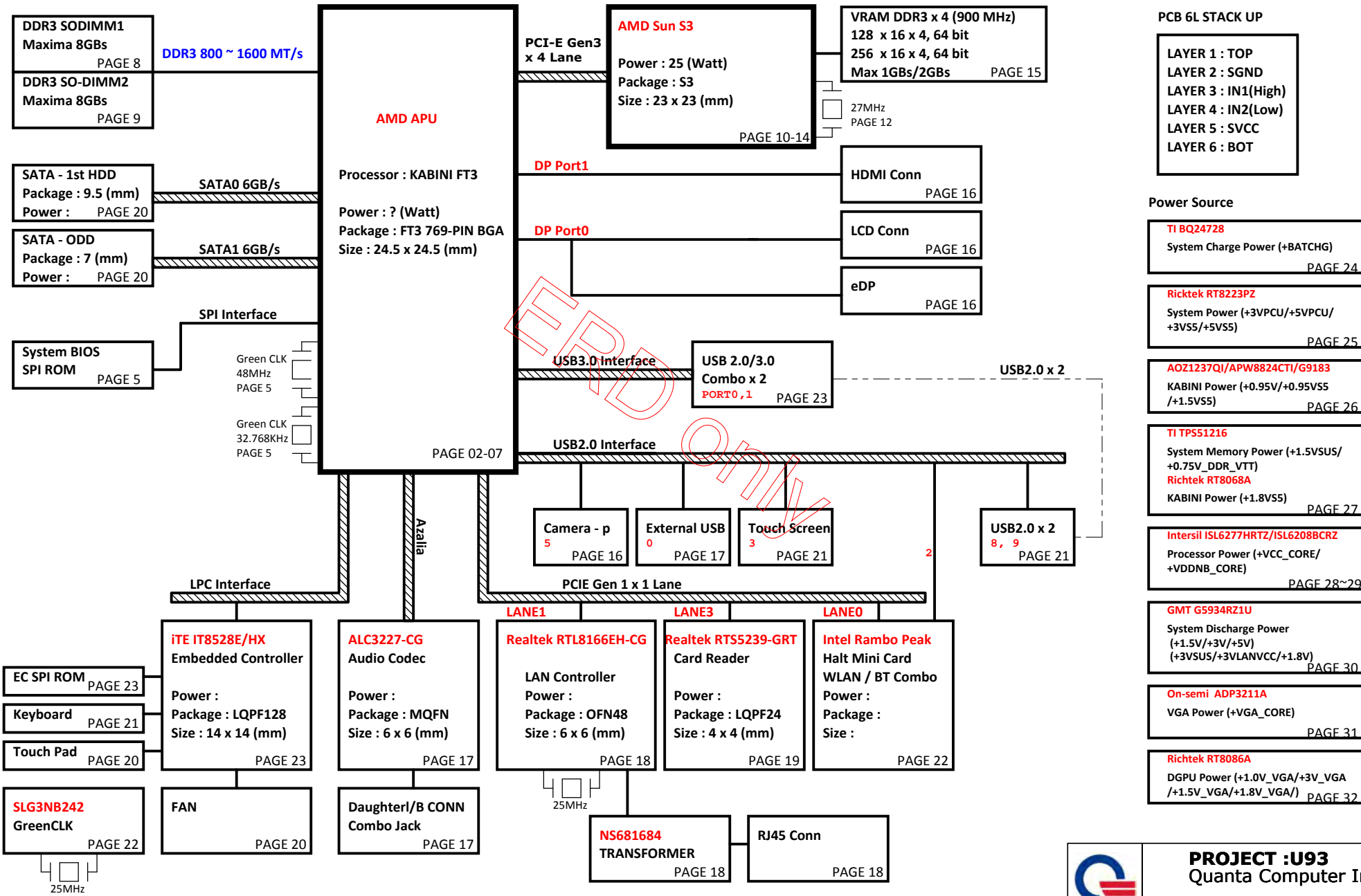
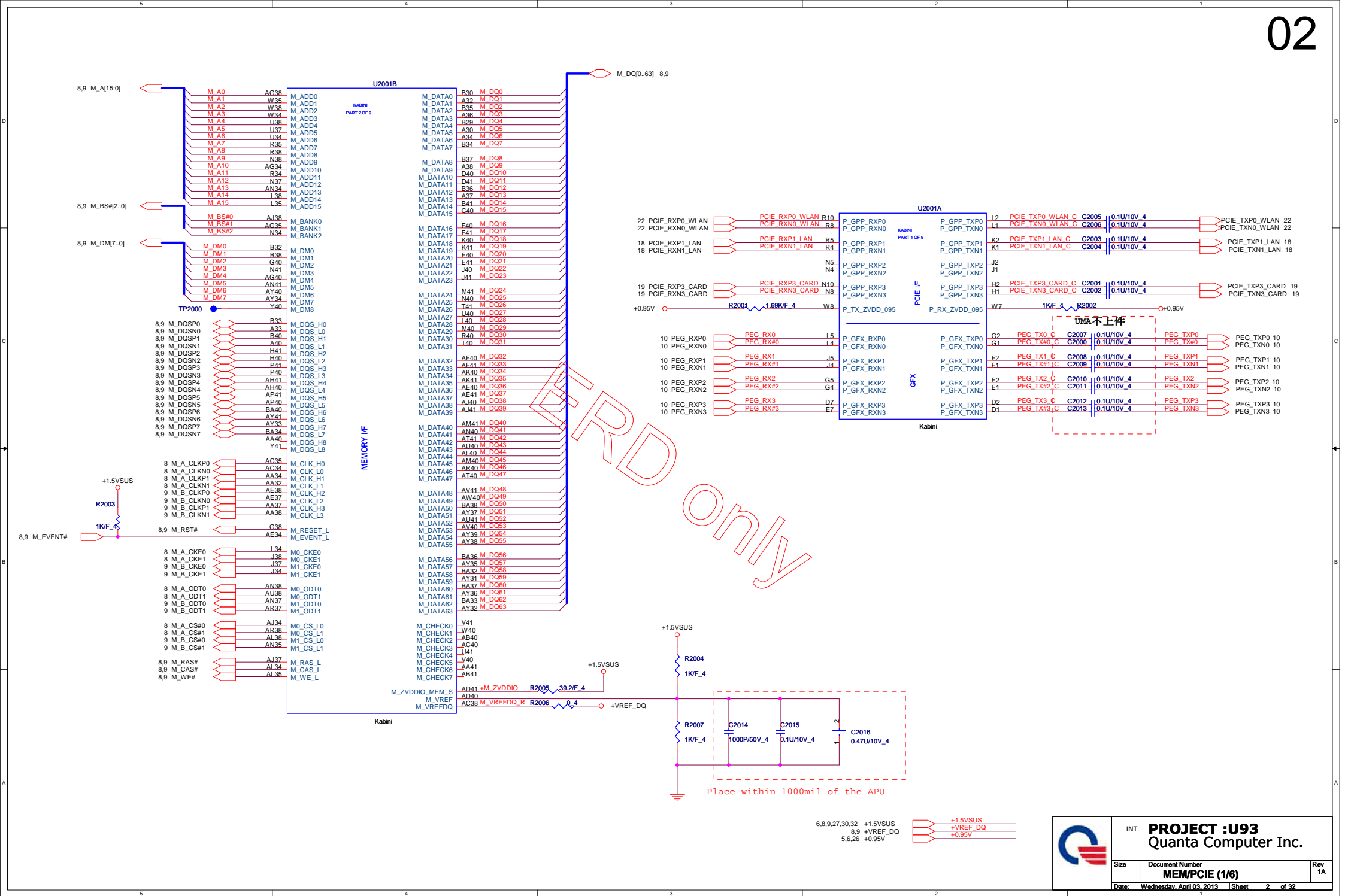


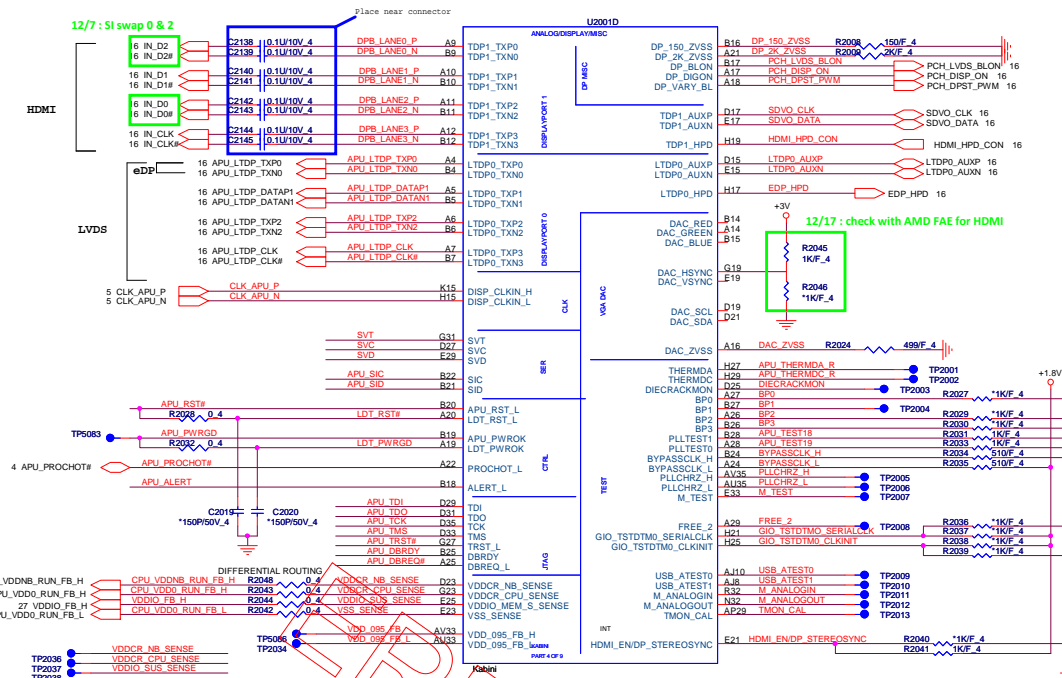
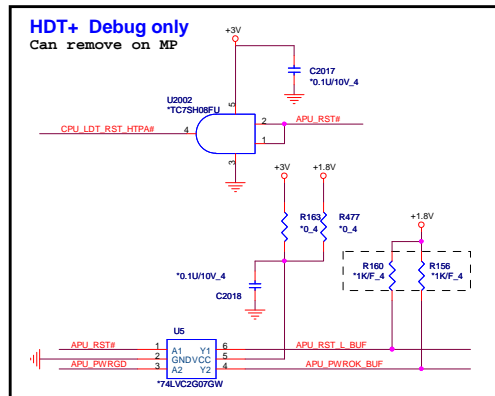
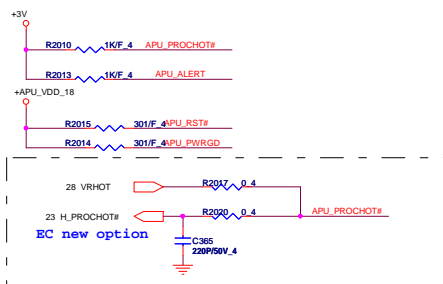
Lean G_AMD KABINI DIS/UMA (14"/15.6")

Ultra/Slim

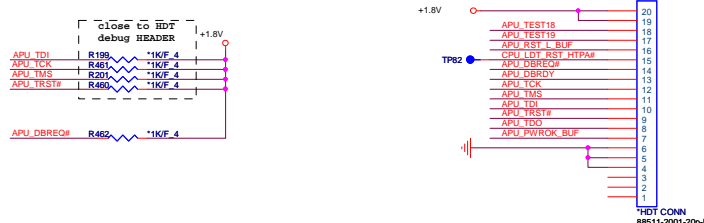
01



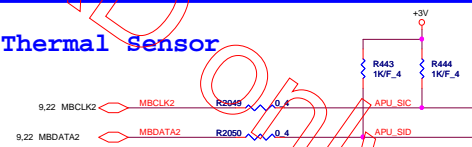




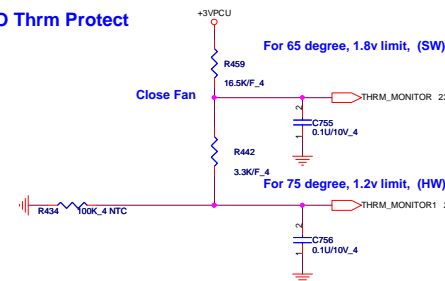
HDT+ Connector for Debug only



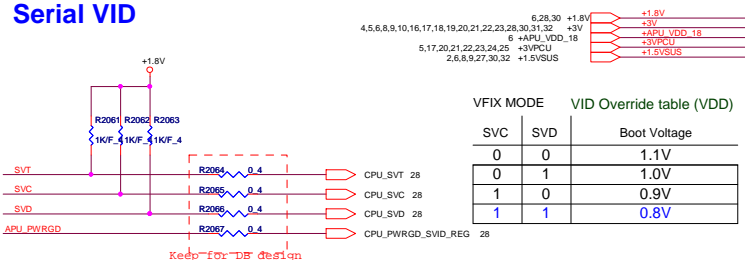
Thermal Sensor



IO Thrm Protect

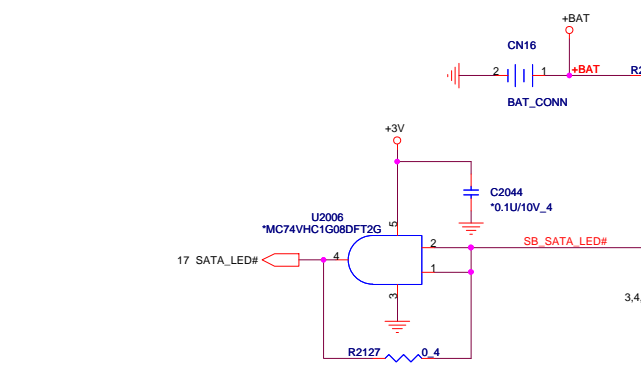
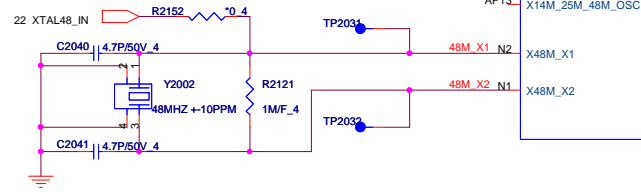
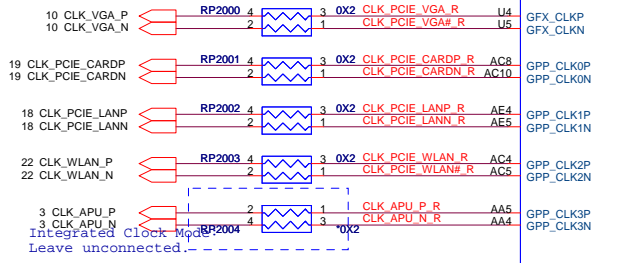
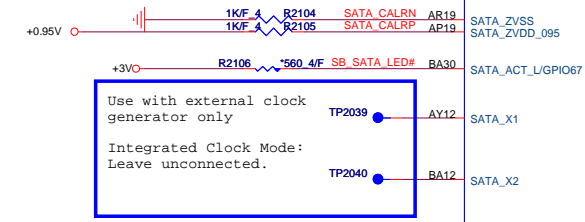
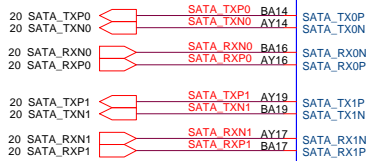


Serial VID



SATA HDD

SATA ODD

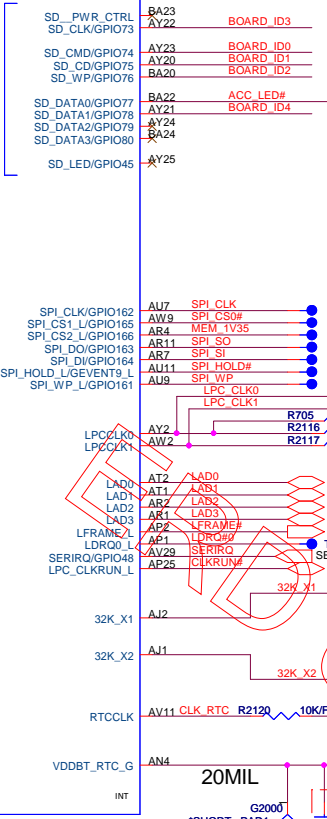


SERIAL ATA

KABINI PART 5 OF 9

SD CARD

SPI ROM



Kabini

INT

20MIL

*SHORT_PAD1

G2000

C2042

0.22U/10V_4

Place C2042 close to PIN

20MIL

3VVRTC

IC AP2138N-1.5TRG1

VOUT

1

+1.5V_RTC

C2149

10U/6.3V_8

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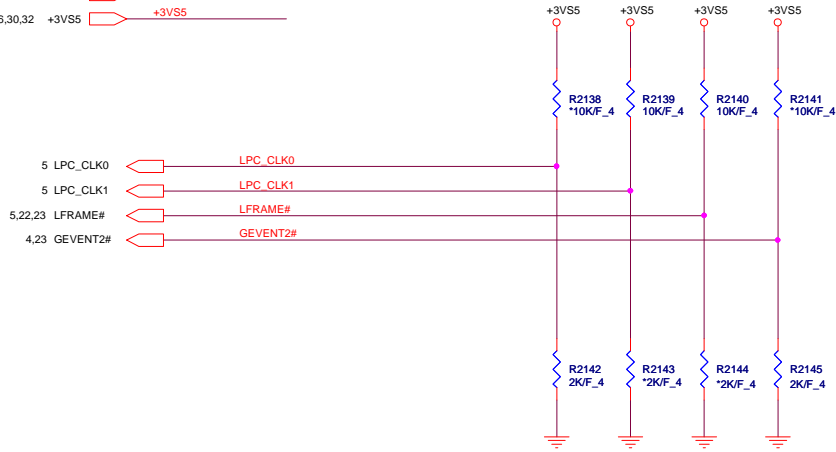
PROJECT :U93
Quanta Computer Inc.

Size	Document Number POWER/GND(5/6)	Rev 1A
Date:	Wednesday, April 03, 2013	Sheet 6 of 32

RAPS PINS

OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

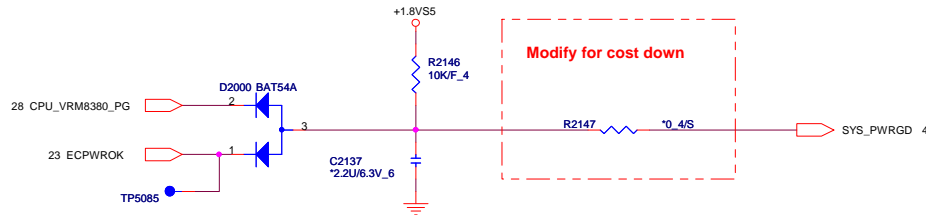
DEBUG STRAPS



REQUIRED STRAPS

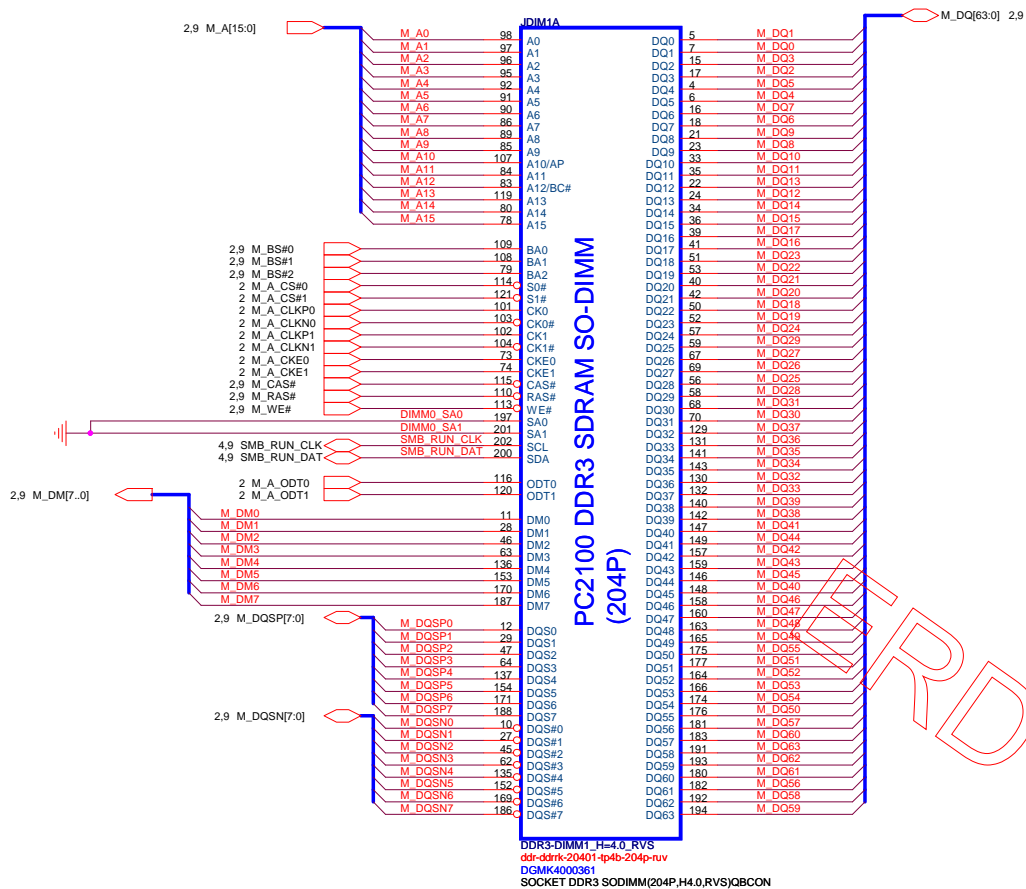
					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

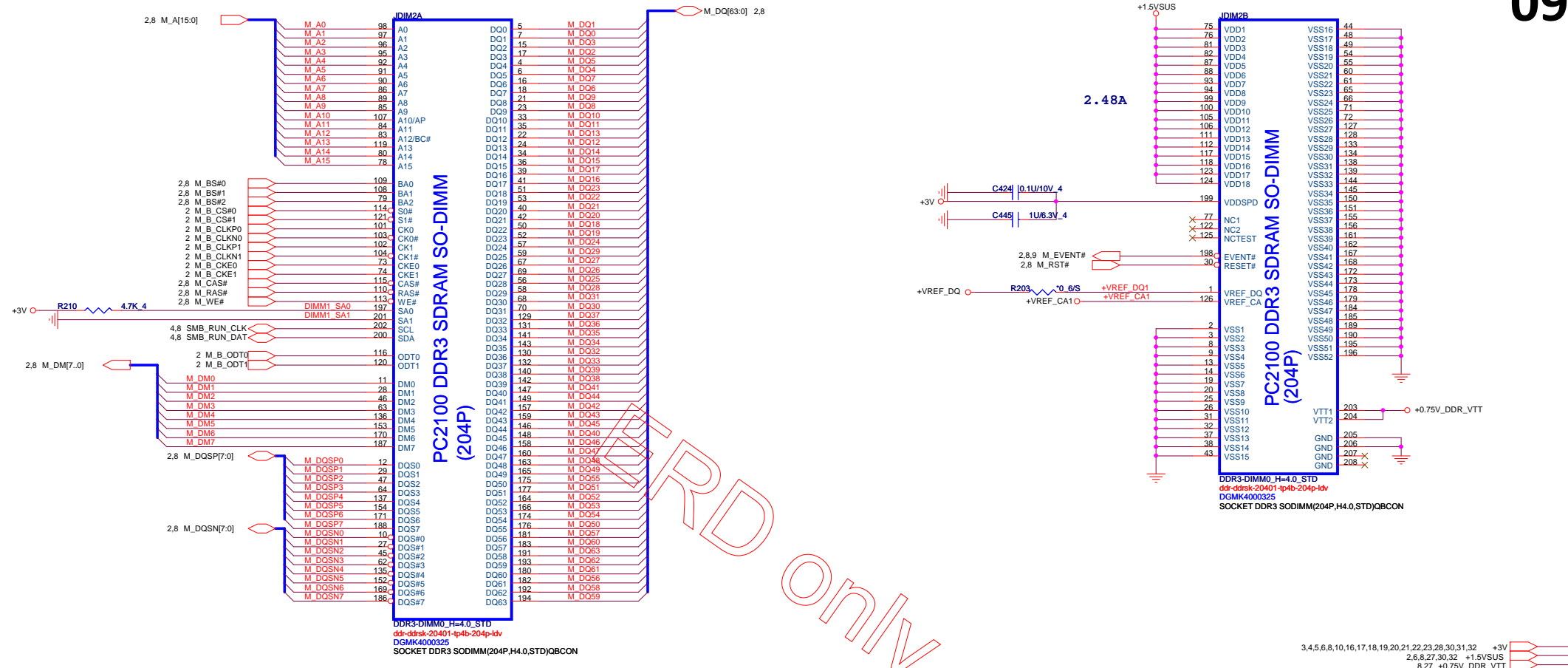
SYS_PWRGD



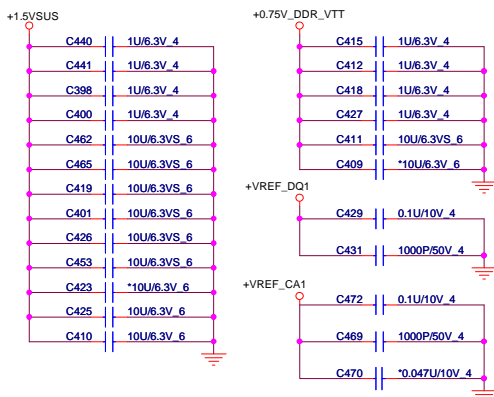
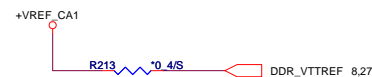
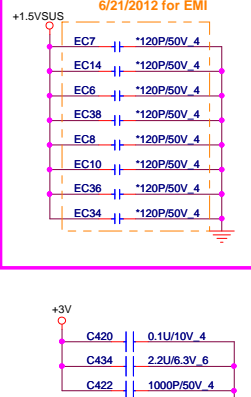
PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
	STRAP (6/6)	1A
Date:	Wednesday, April 03, 2013	Sheet 7 of 32



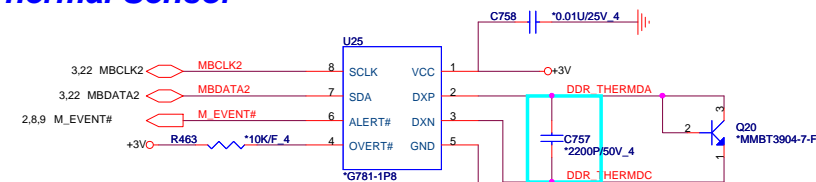


Place these Caps near So-Dimm1.

For EMI RESERVE
6/21/2012 for EMI

Local Thermal Sensor

DDR3 Thermal Sensor

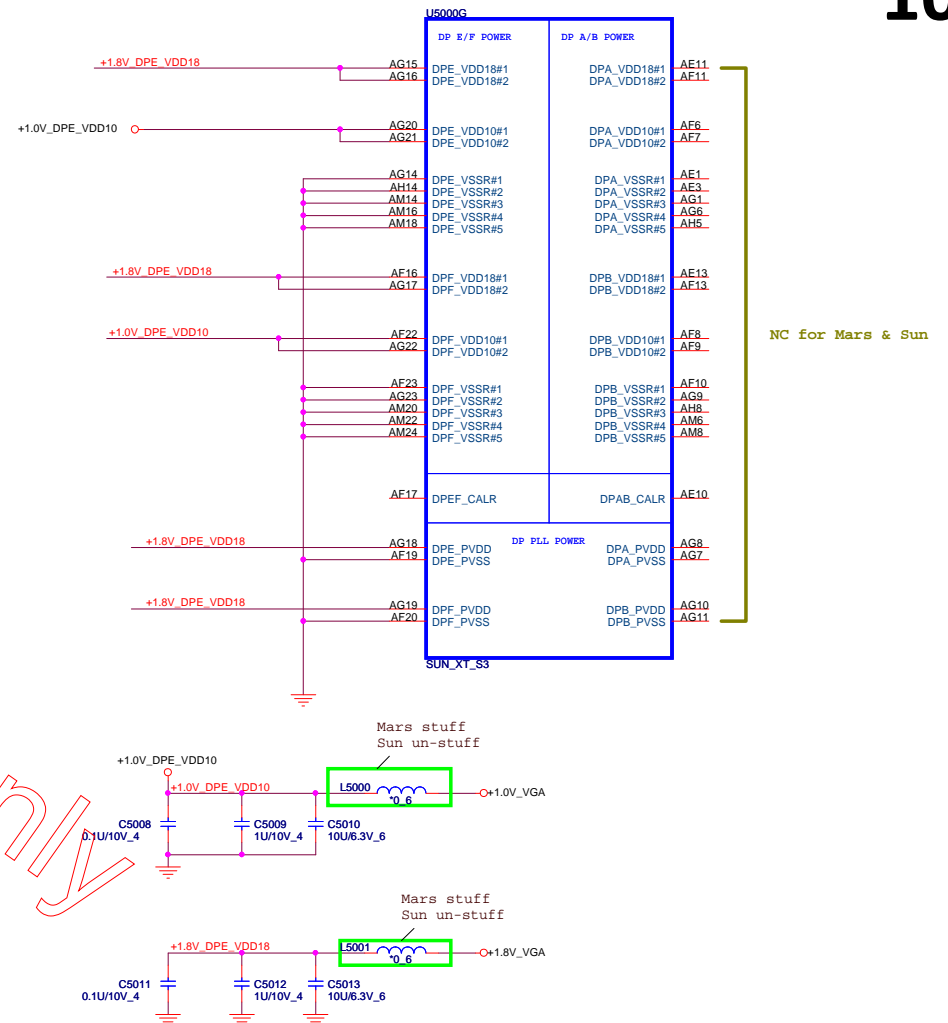
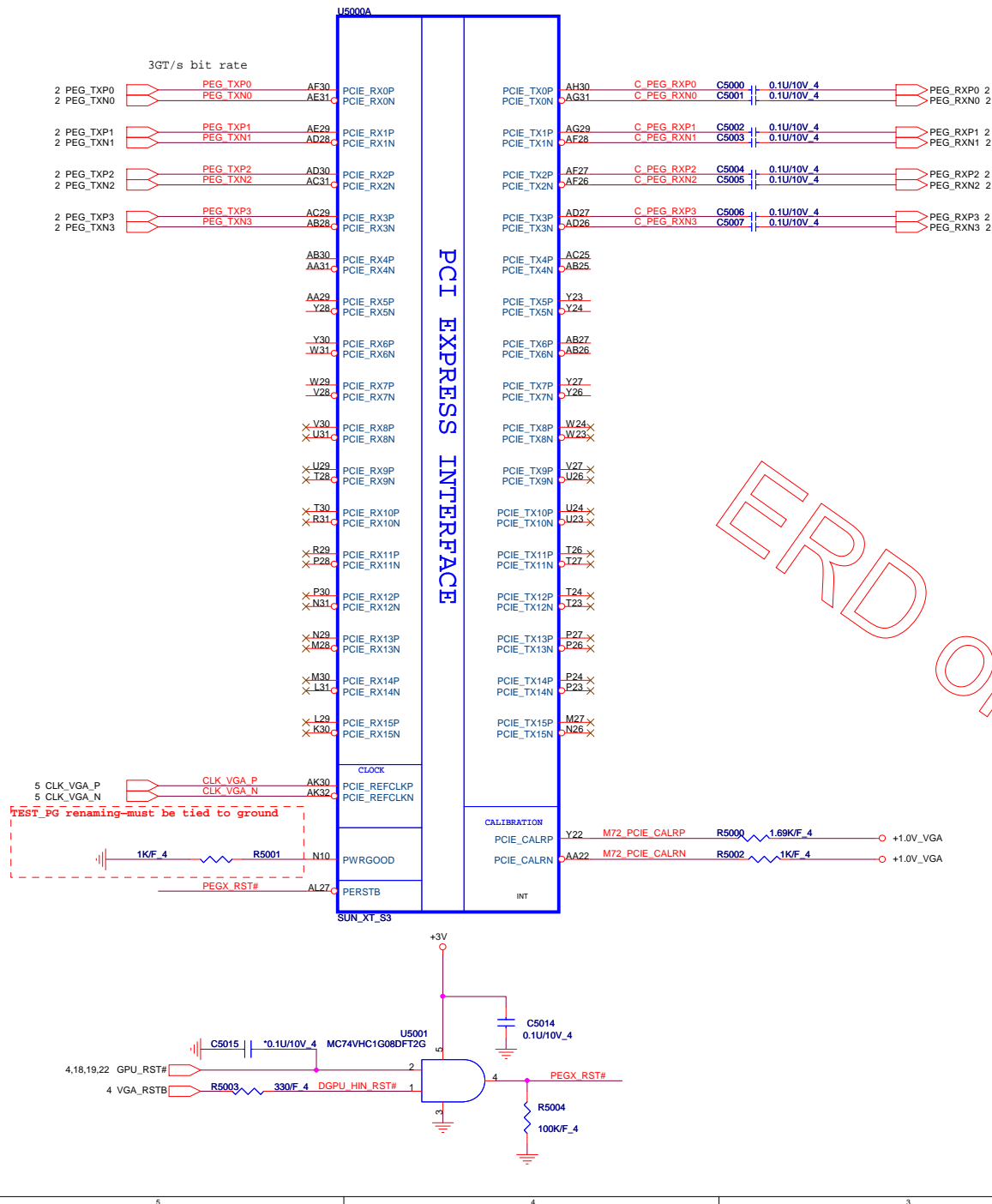


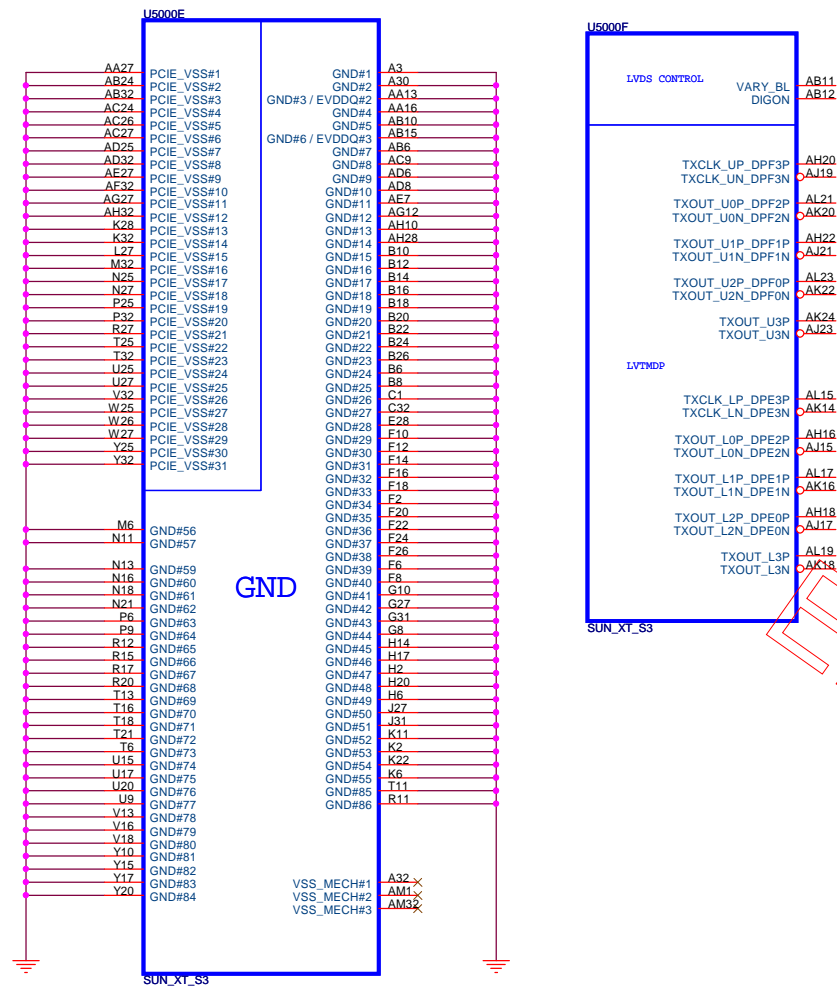
If use internal thermal IC, C9007 use 0ohm.

Main:AL000781039 G781-1P8(9Ah)
 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

PROJECT :U93		
Quanta Computer Inc.		
Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A
Date: Wednesday, April 03, 2013	Sheet 9 of 32	





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

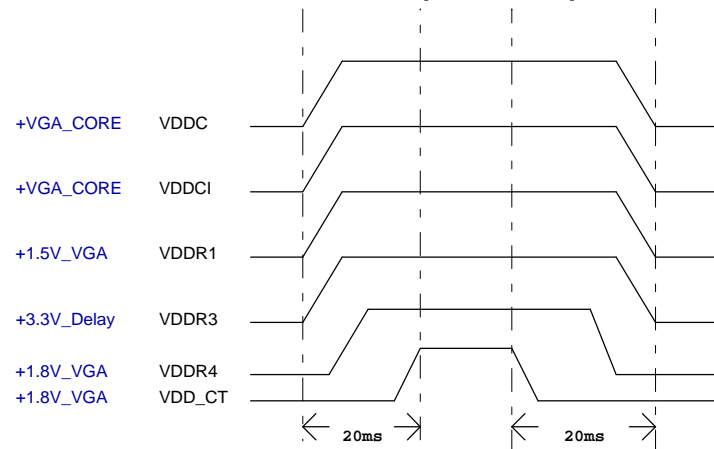
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIOQ[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUDI[1] AUDI[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED,
THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

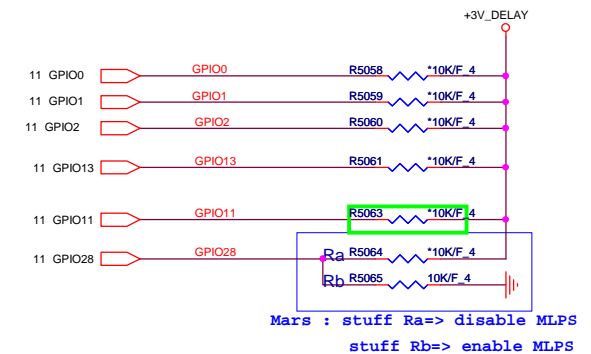
Power Up/Down Sequence



Memory Aperture size(Seymour)

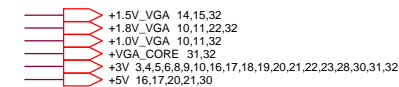
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

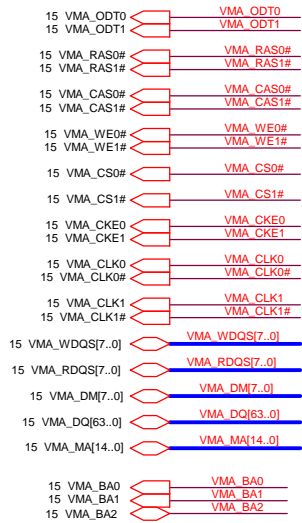
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



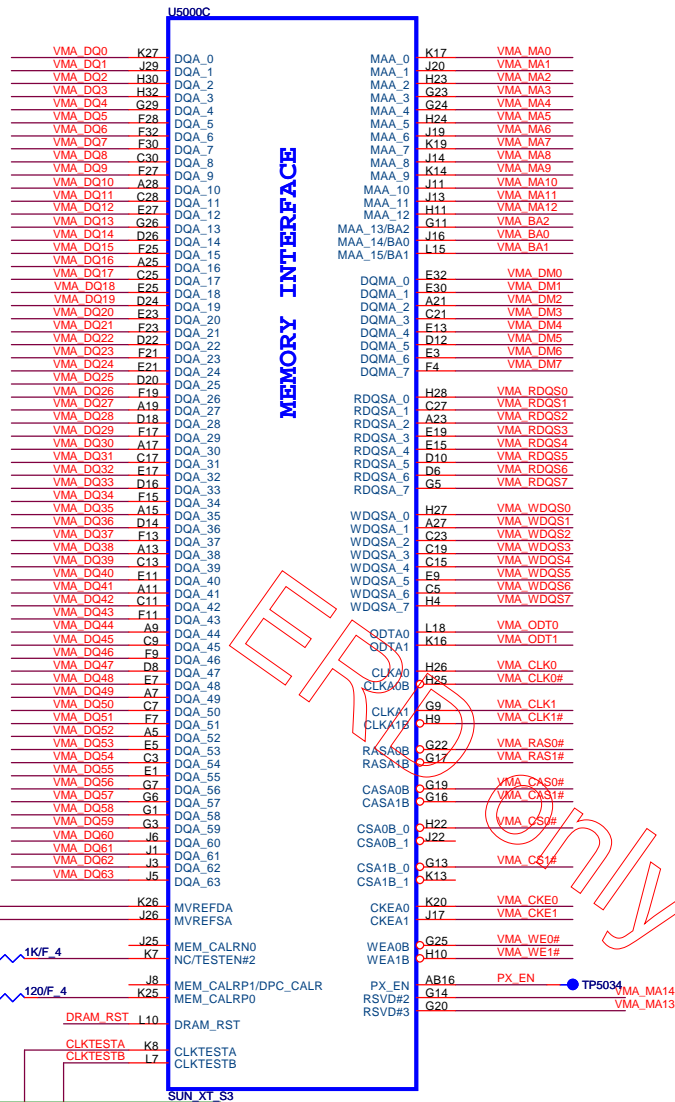
PROJECT :U93
Quanta Computer Inc.

Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
Date: Wednesday, April 03, 2013	Sheet 12 of 32	

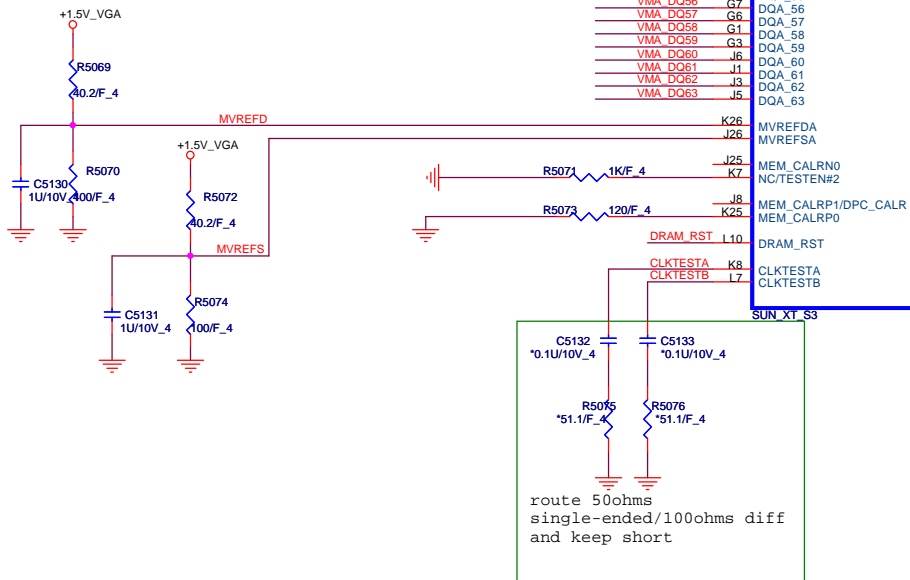
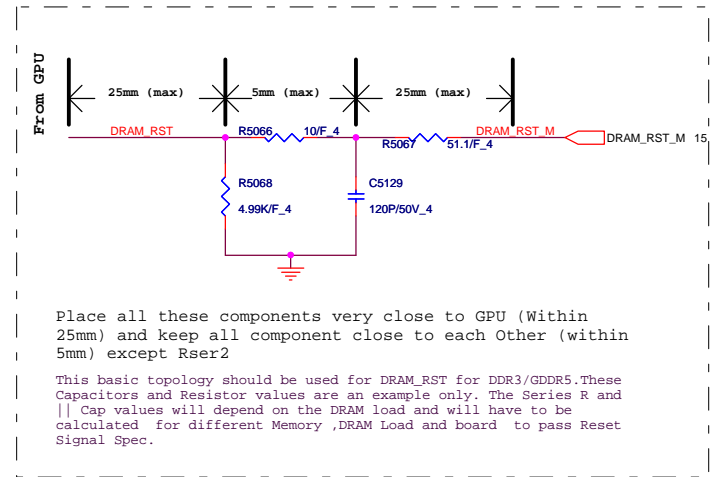




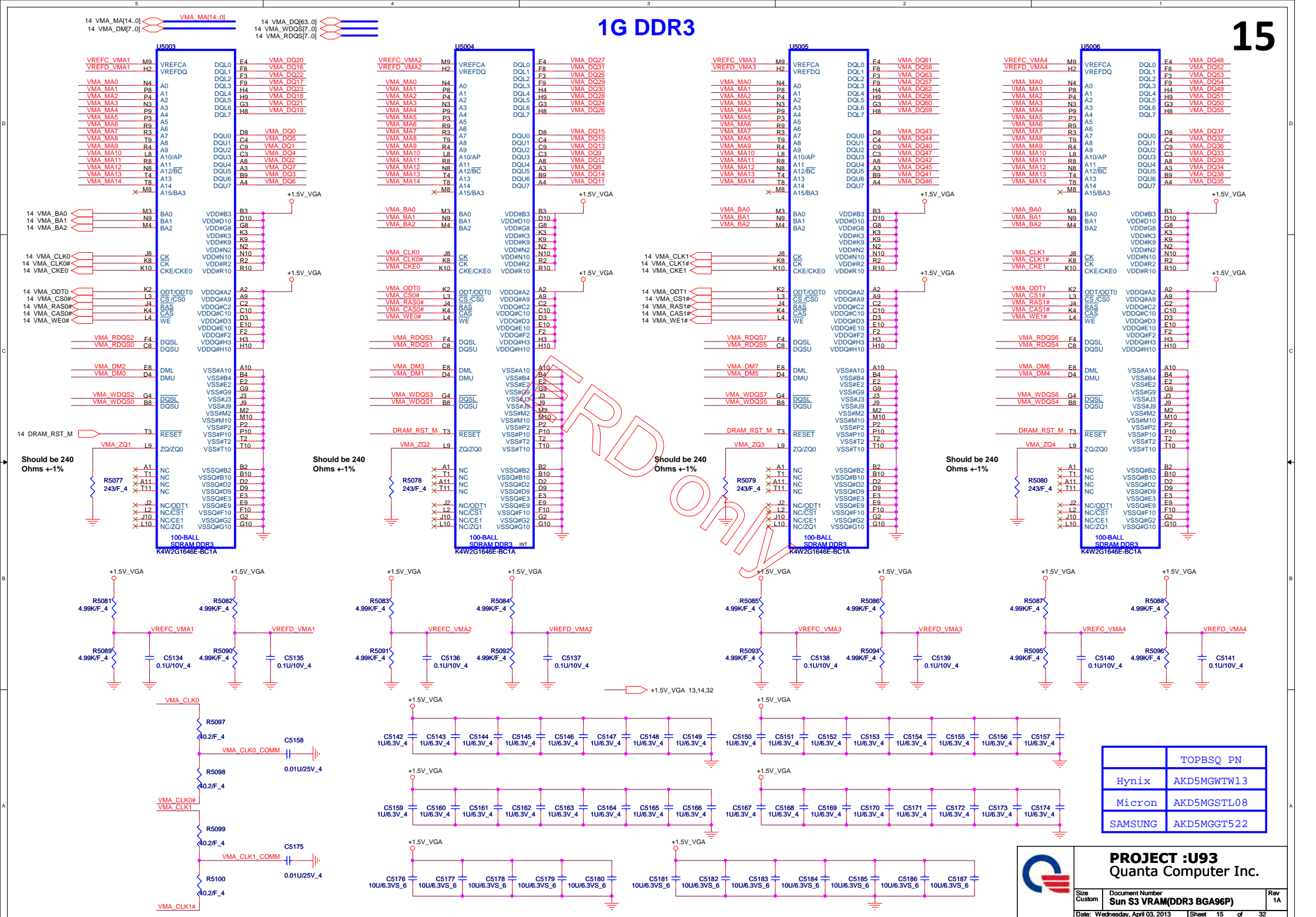
support 1gbt
VRAM (64M X 16)



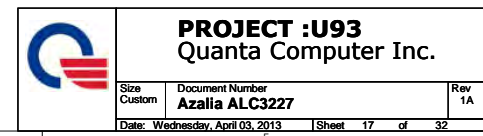
MEMORY INTERFACE



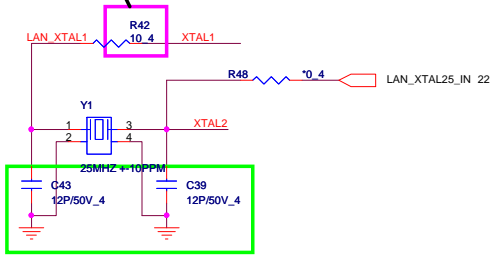
PROJECT :U93
Quanta Computer Inc.



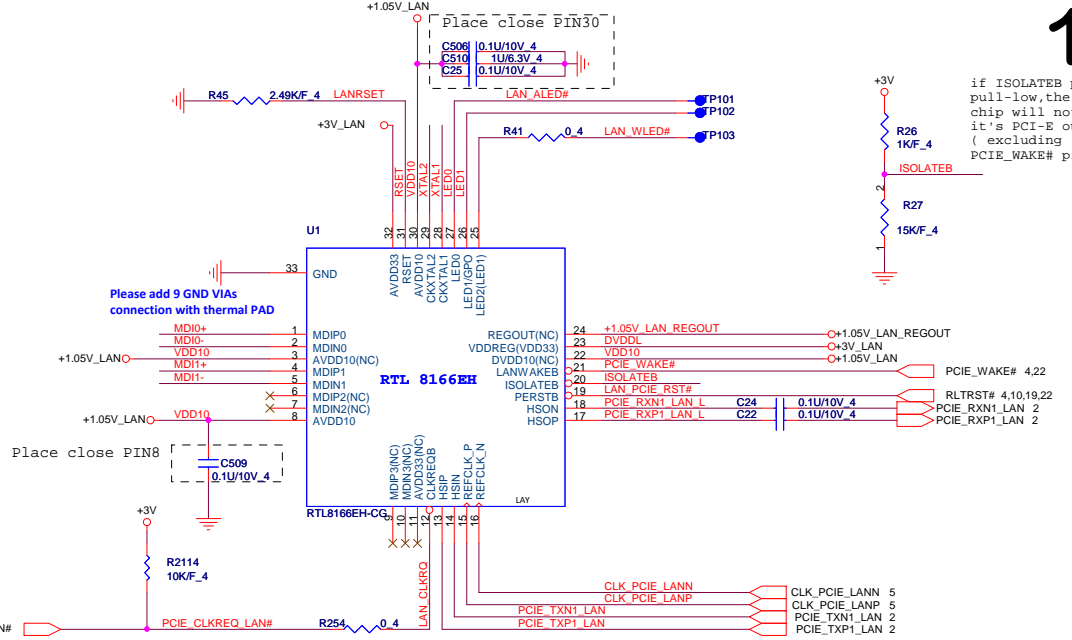
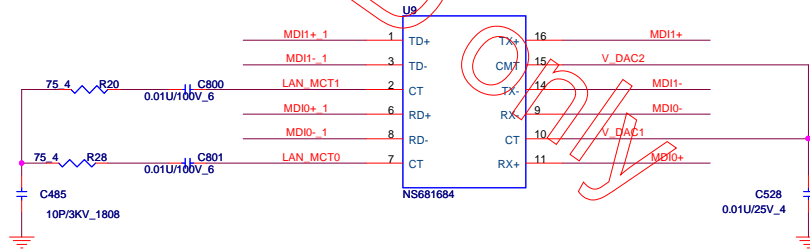
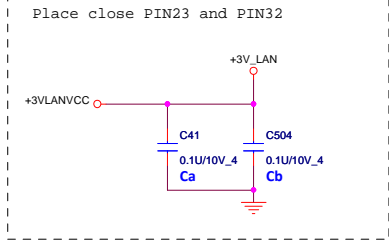
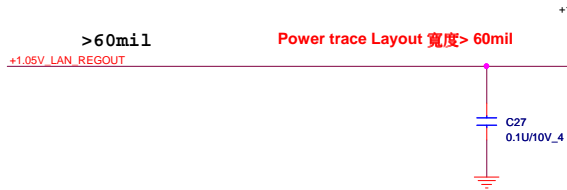
	TOPBSQ PN
Hynix	AKD5MGWTW13
Micron	AKD5MGSTL08
SAMSUNG	AKD5MGGT522



For EMI 0 ~ 22 ohm

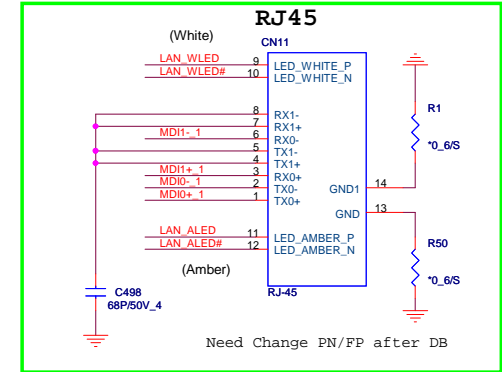


SI change to 12p

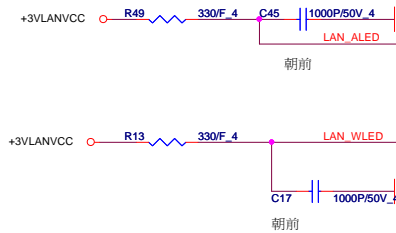


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

LAN conn



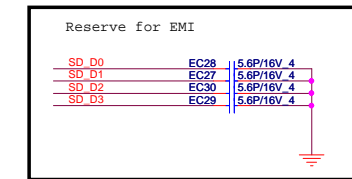
Need Change PN/FP after DB



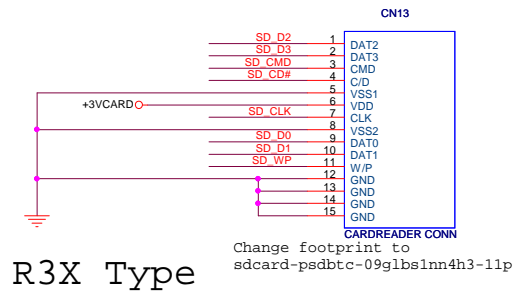
3,4,5,6,8,9,10,16,17,19,20,21,22,23,28,30,31,32 +3V
22.30 +3V_LANVCC

SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

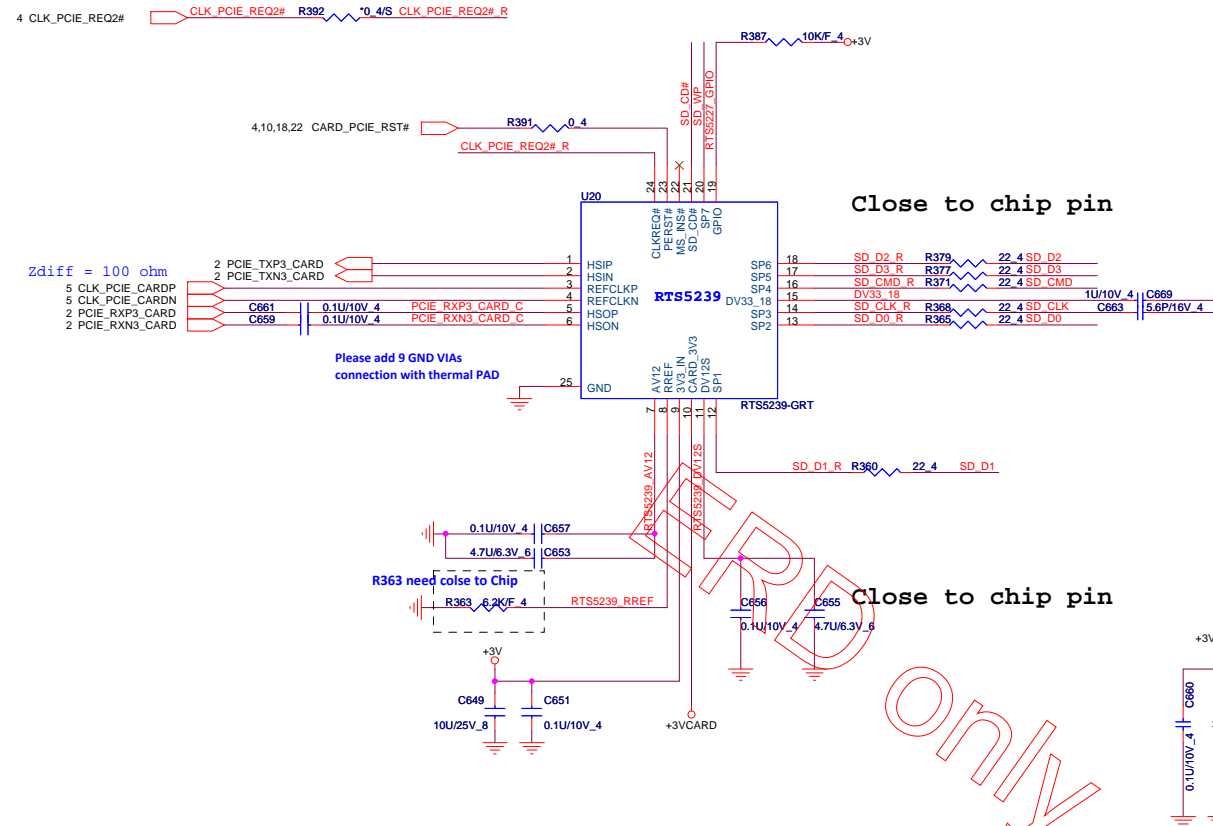
Share Pin



SD / MMC
CARD READER

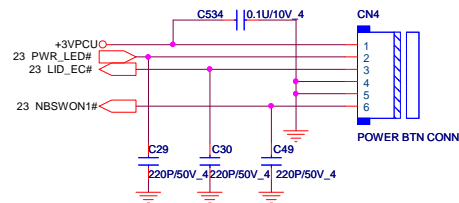


R3X Type

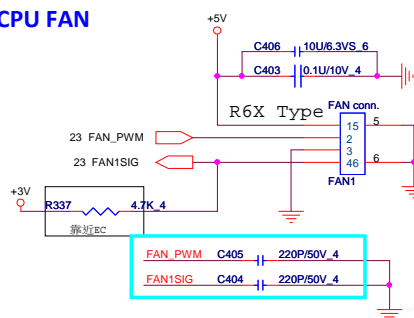


Power Button Connector

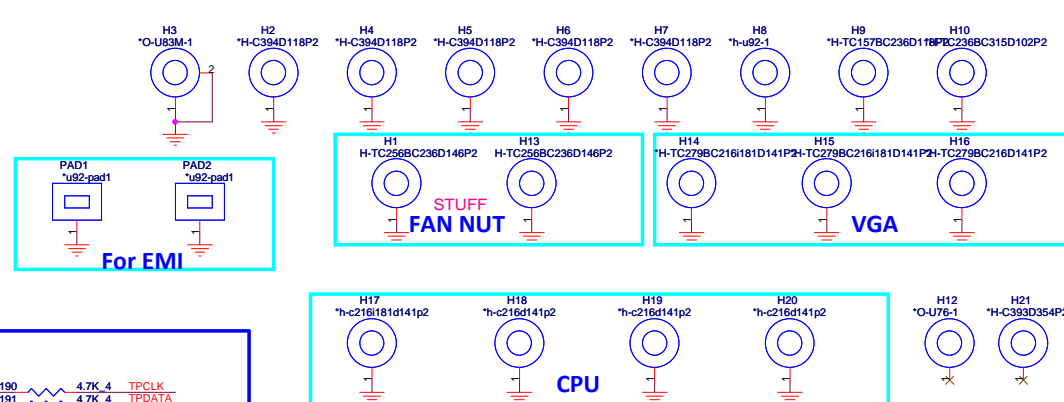
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



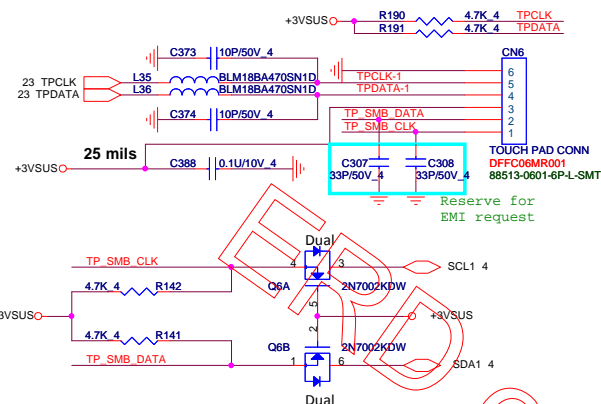
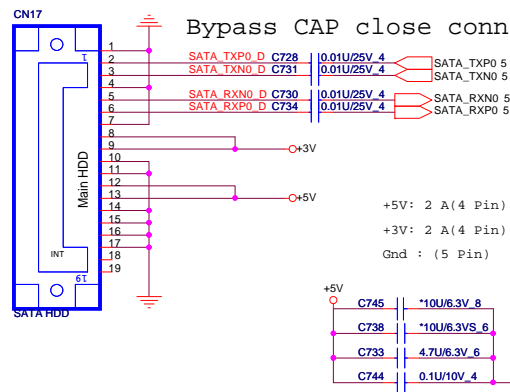
CPU FAN



Hole

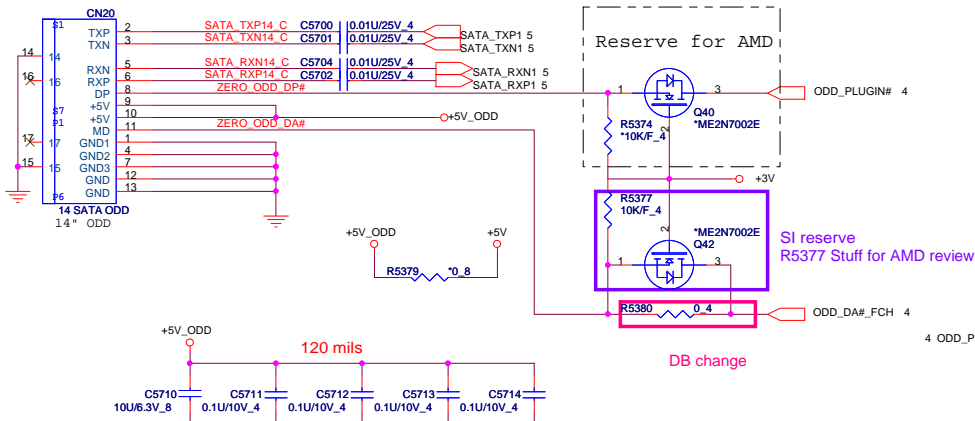


SATA HDD Connector(Cable type)



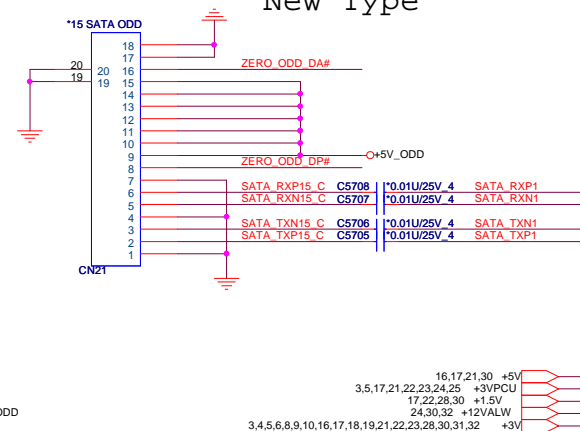
SATA ODD CONNECTOR

14" SATA ODD Bypass CAP close conn



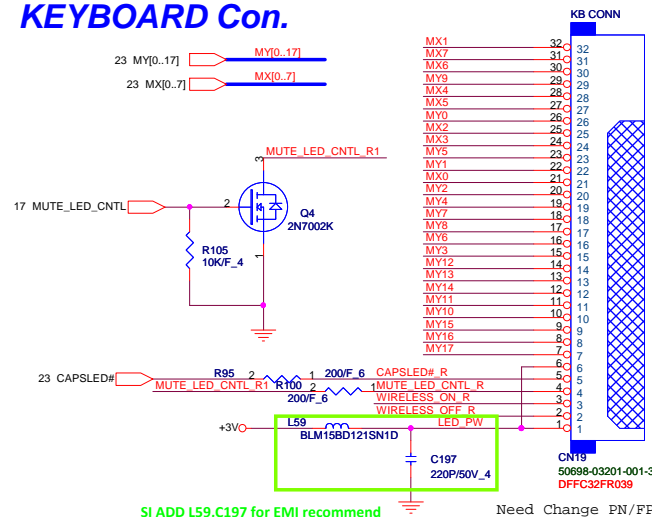
15" SATA ODD

New Type

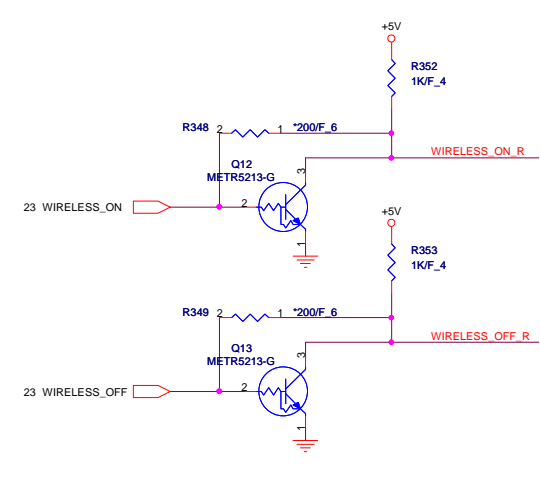
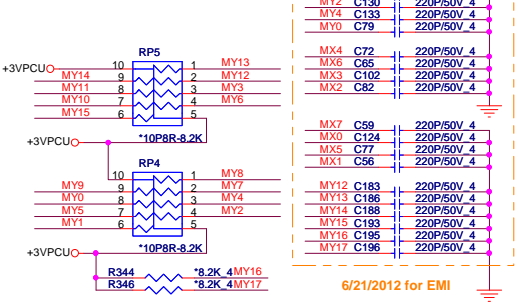


KEYBOARD Con.

21

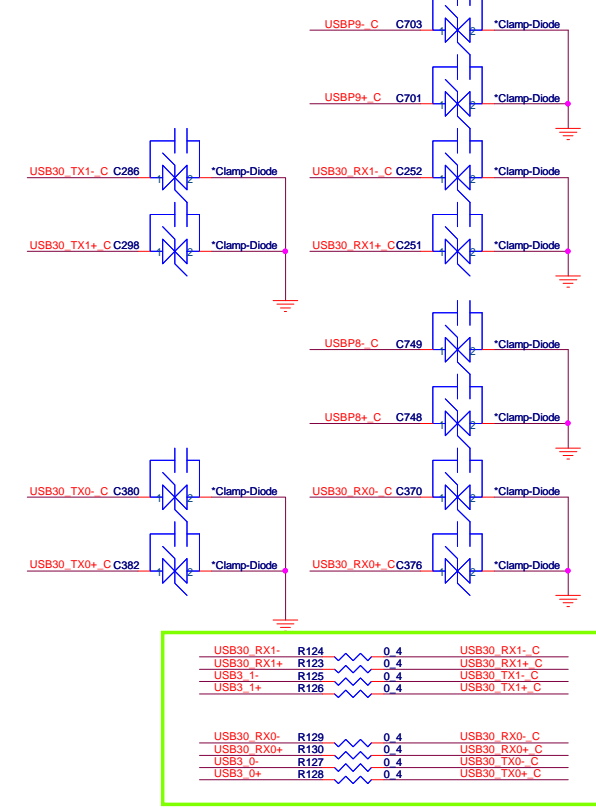


KEYBOARD PULL-UP



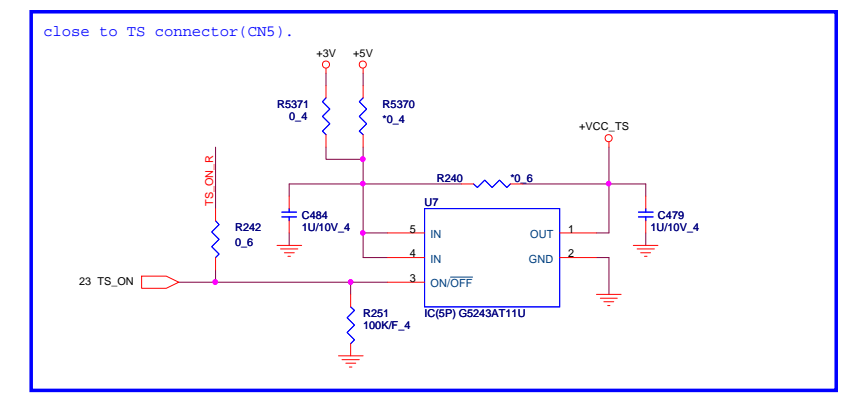
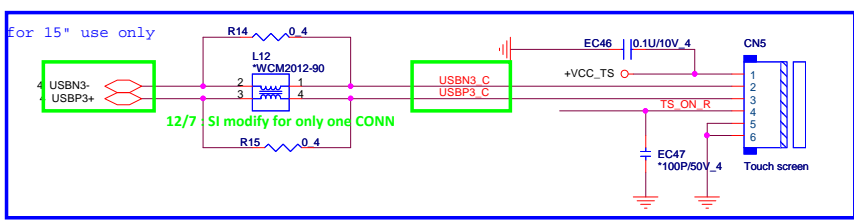
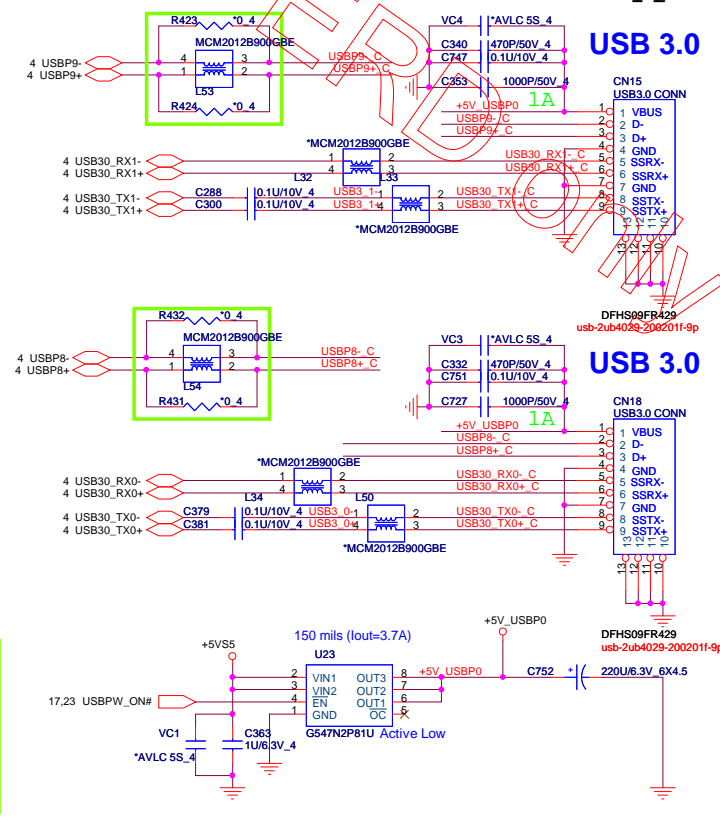
NM9 Type

USB 2.0/3.0 Combo



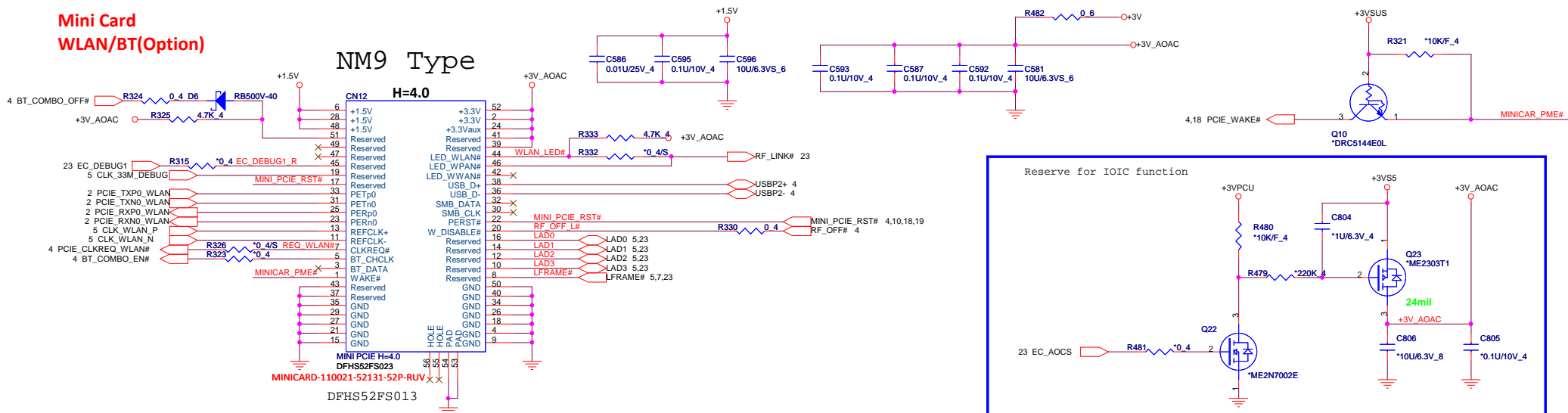
SPS Type

USB 3.0

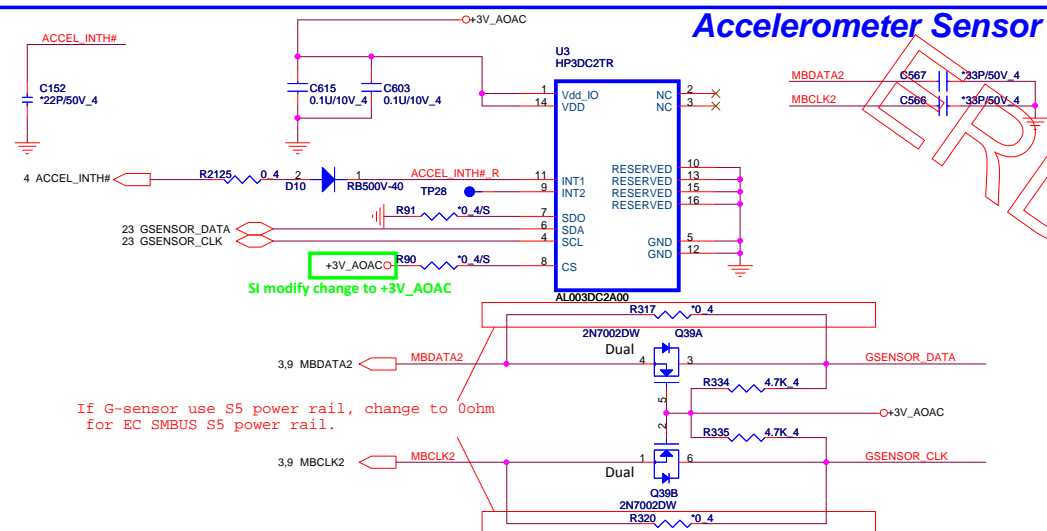


Mini Card WLAN/BT(Optional)

NM9 Type

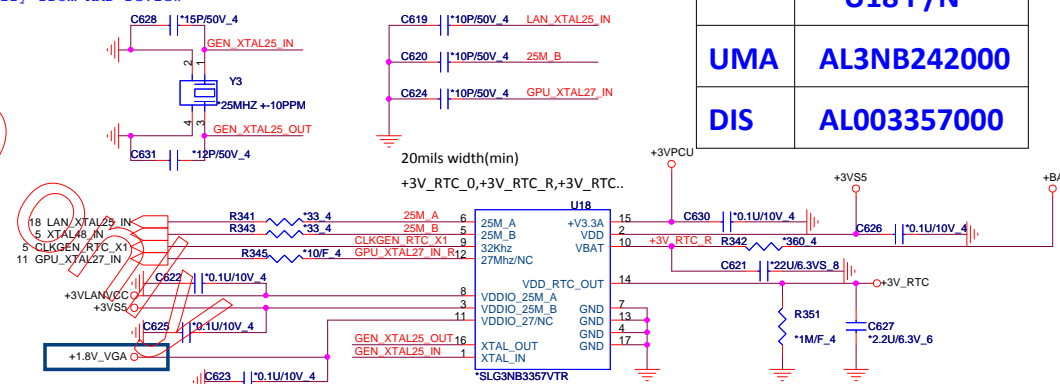


Accelerometer Sensor



Green CLK Circuitry

Modify from AMD review

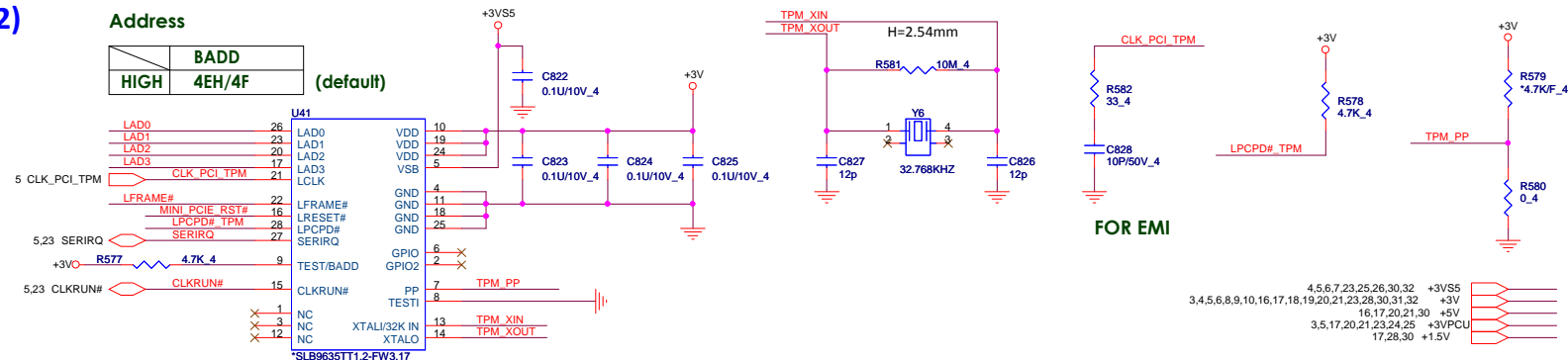


U18 P/N	
UMA	AL3NB242000
DIS	AL003357000

TPM (1.2)

Address

Address	Value
BADD	4EH/4F (default)

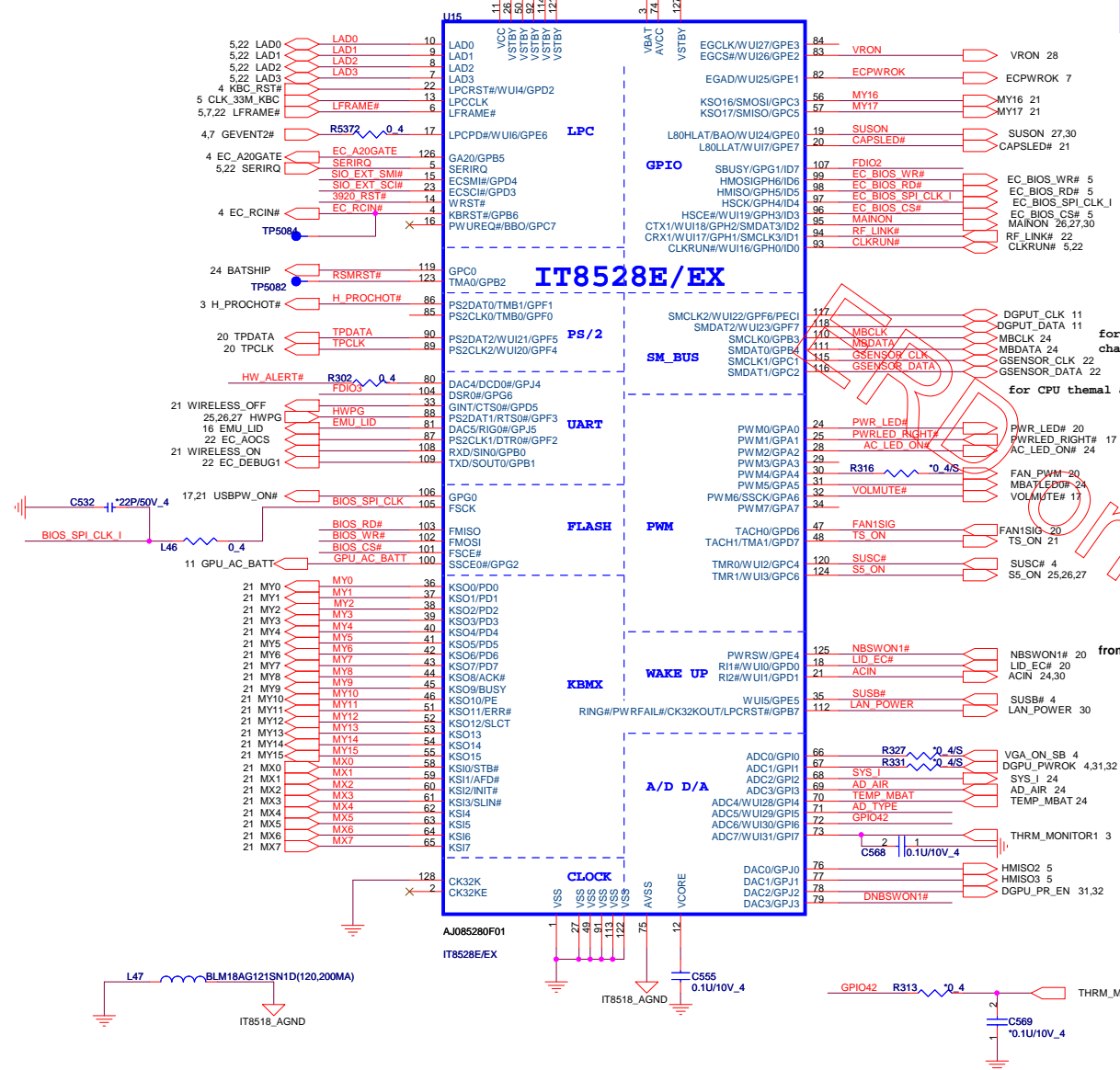


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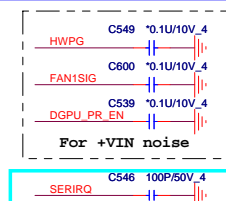
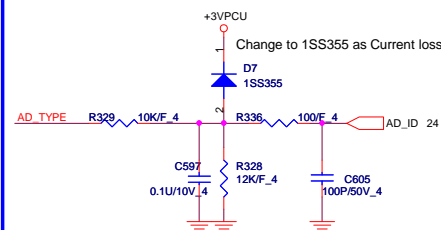
Size	Document Number	Rev
Custom	MINI-PCIE/LED	1A
Date: Wednesday, April 03, 2013	Sheet	22 of 32

3,4,5,6,8,9,10,16,17,18,19,20,21,22,28,30,31,32 +3V
3,5,17,20,21,22,24,25 +3VPCU

ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode

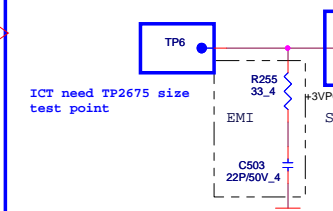
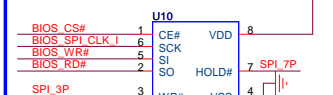


Smart adapter Type check

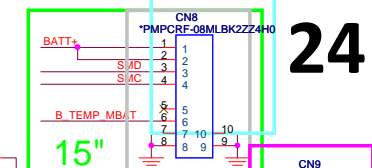


Vender	Size	P/N
AIT	4M	AKE39ZN0800
GGD	4M	AKE39GN0Q01
WND	4M	AKE39FN0N01
Socket		DFHS08FS023

4M SPI EC ROM

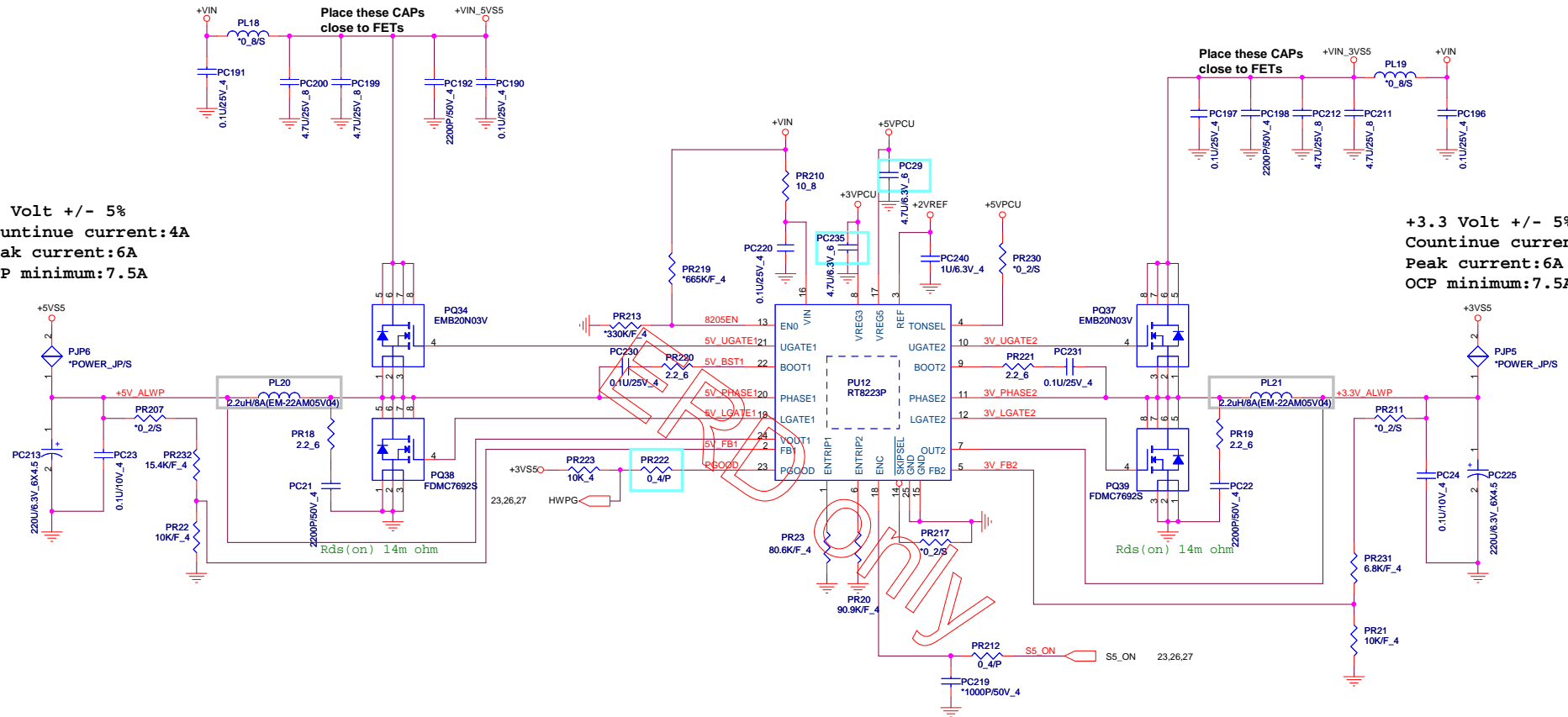


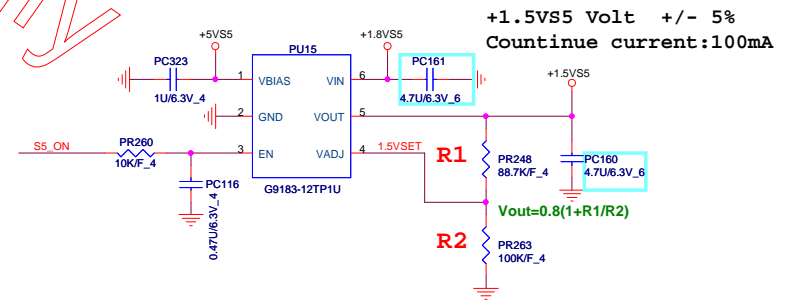
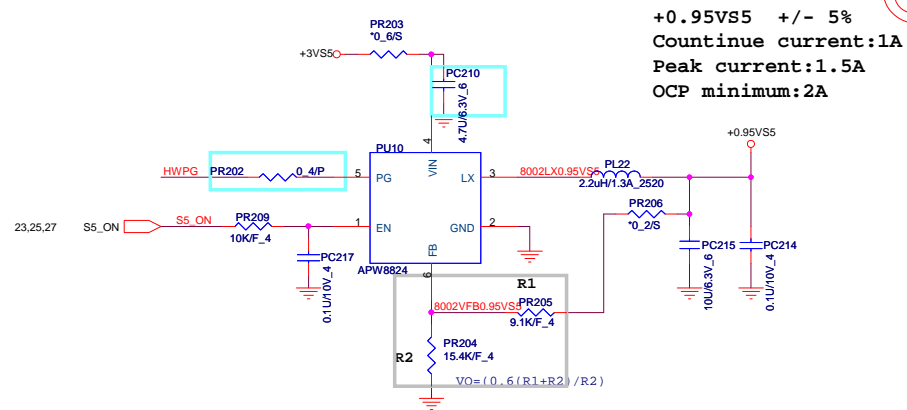
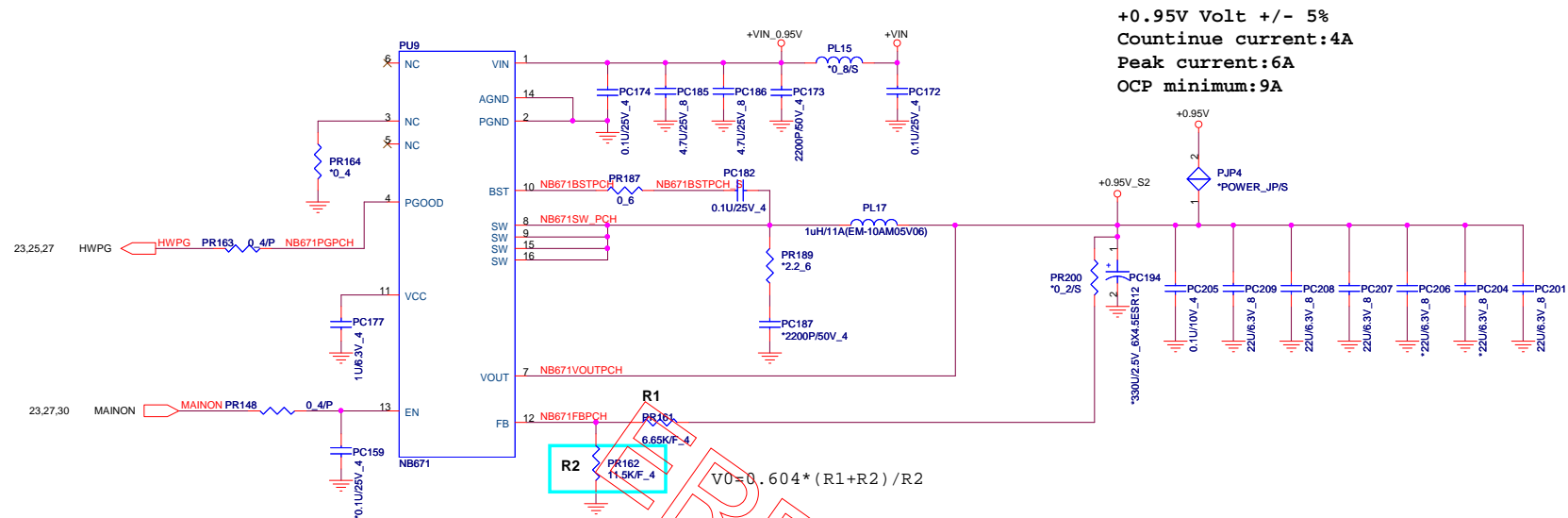
DGPU Thermal protect

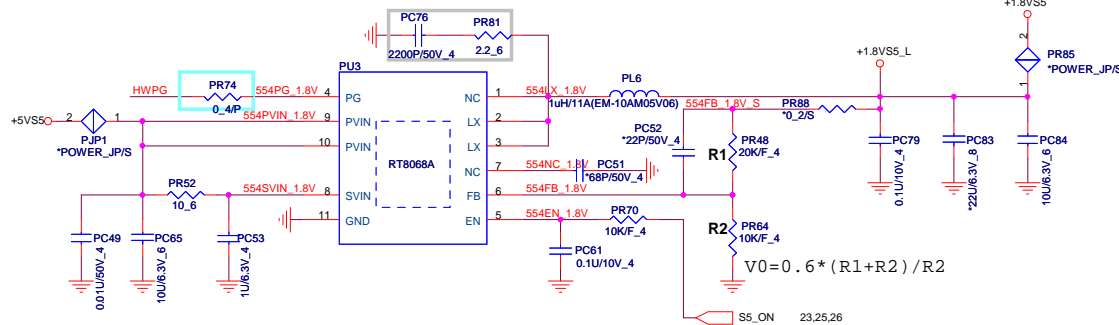
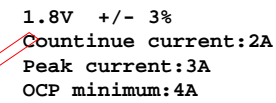


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

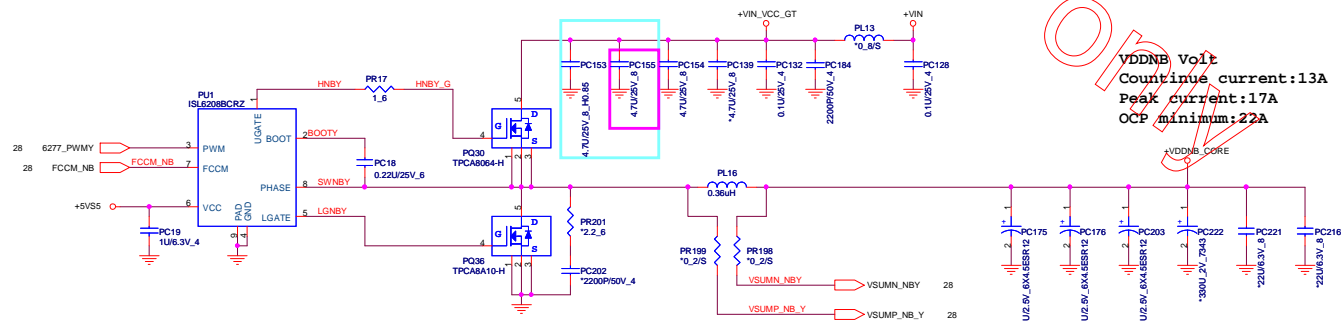
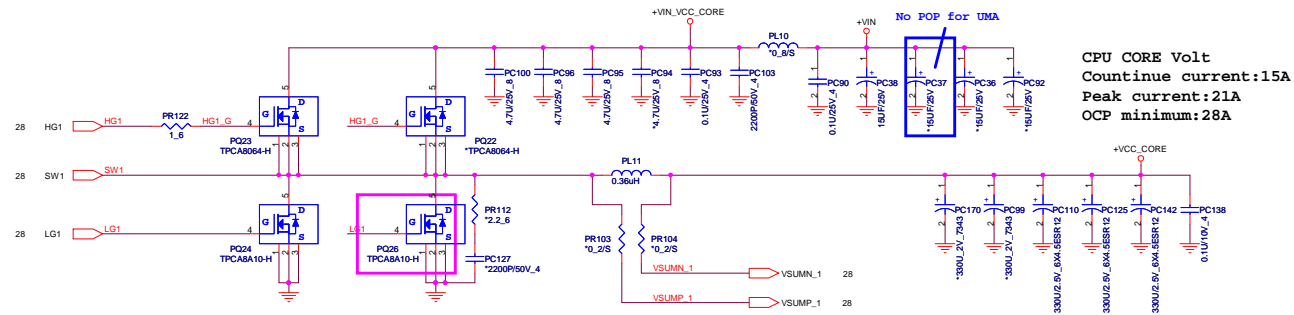
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A







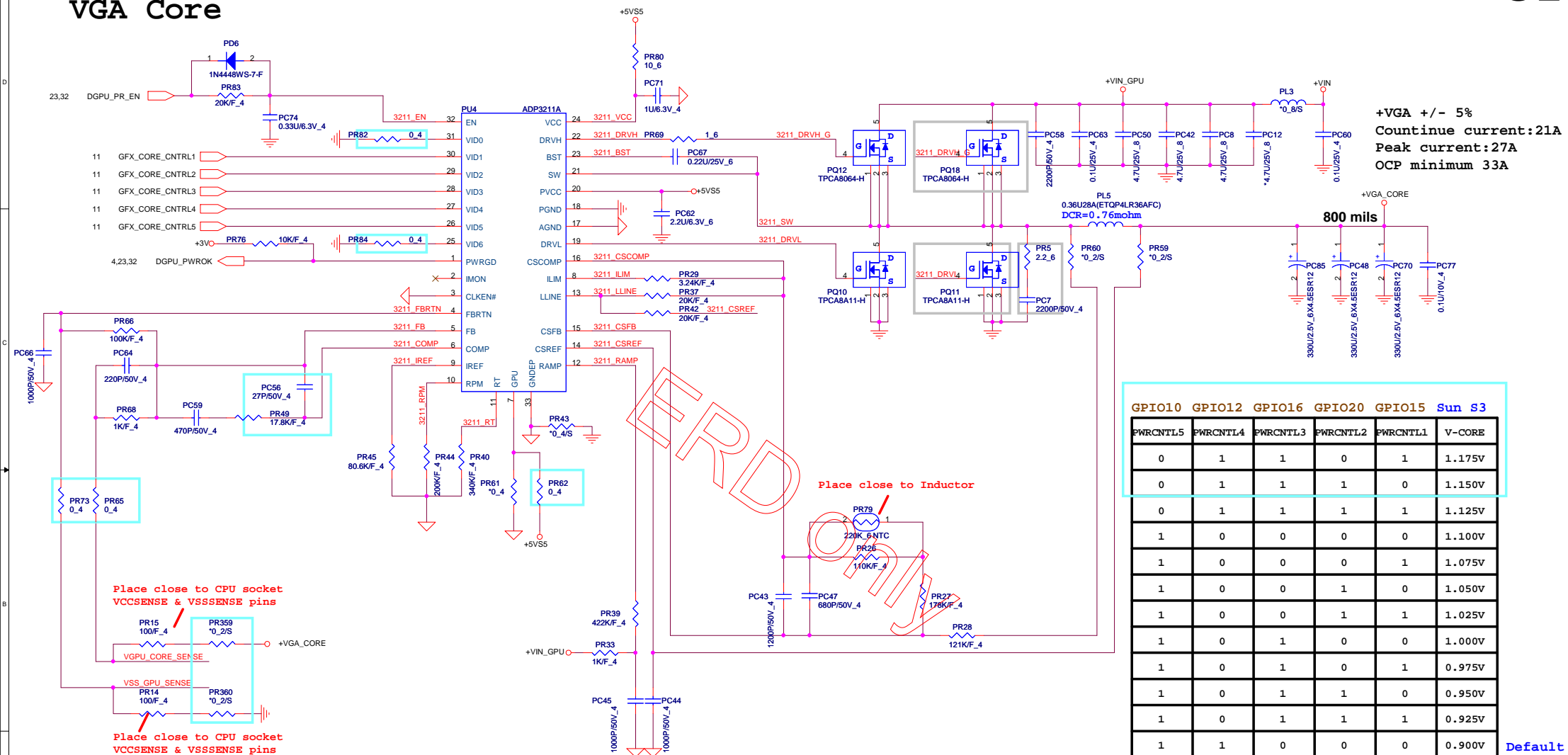
Size Custom	Document Number DDR3 (TPS51216)	Rev 1A
Date: Wednesday, April 03, 2013		Sheet 27 of 32



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Site Custom	Document Number ISL6208	Rev 1A
Date: Wednesday, April 03, 2013 Sheet 29 of 32		

VGA Core

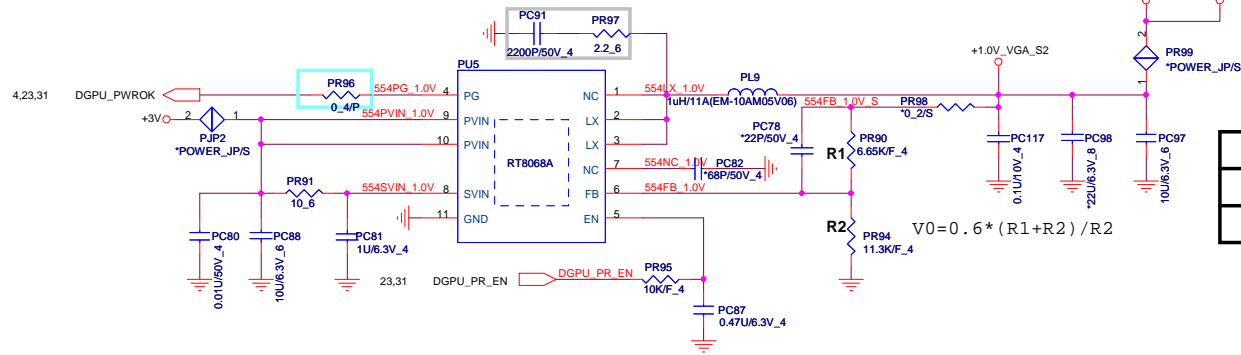


+VGA +/- 5%
Countinue current:21A
Peak current:27A
OCP minimum 33A

800 mils

Default

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

